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EXAMINER	
JOHNSON, BRIAN P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/785,671	NAKAJIMA, HIROYUKI	
	Examiner	Art Unit	
	BRIAN P. JOHNSON	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *23,24,26-36,41,42 and 47-50* is/are pending in the application.

4a) Of the above claim(s) *20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23,24,26-36,41,42 and 47-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/27/08; 1/13/06; 3/18/04; 2/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 23, 24, 26-36, 41, 42, and 47-50 have been examined. Claim 20 has been withdrawn from consideration.

2. Acknowledgement of papers filed: remarks and amendments filed on 12 June 2008. These papers filed have been placed on record.

Continued Examination Under 37 CFR 1.114

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12 June 2008 has been entered.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 27, 29, 30, 31, 32, 34 and 50 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 27: lack of antecedent basis for "the first processing unit."

Claim 28: lack of antecedent basis for "the first processing unit" and "the second processing unit"

Claim 29: lack of antecedent basis for "said first pipeline" and "said second pipeline" (first and second pipeline stages could be in the same pipeline the way it is claimed). Could be fixed by adding "a first pipeline comprising/having" at the beginning of line 2 of claim 28 and "a second pipeline comprising/having" at the beginning of line 3."

Claim 29: it is unclear what the first pipeline has a different number of.

Claim 30: lack of antecedent basis for "said stage number" and "the pipeline"

Claim 31: lack of antecedent basis for "the first and second pipeline"

Claim 32: it is unclear how a system instruction decoder selects the use of the first and second decoder. This is particularly confusing when claim 33 indicates that the system instruction decoder is separate from the first and second decoders. It is unclear whether this is a discrepancy or whether Claim 32 is a separate embodiment of the invention where a decoder somehow selects the use of two other decoders.

Claim 50: the claim is confusing as written. Please consider using labels less ambiguous than “another node” and “yet another node.” The use of, for example, a "first node" and "second node" would be much clearer.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 23, 24, 26-31, 34, 36, 41, 42, and 47-50 are rejected under 35 U.S.C. 102(b) as being anticipated by Miller (U.S. Patent No. 6,081,884).

9. Regarding claim 23, Miller discloses a processor that performs a first instruction set (Fig.3 RISC) and a second instruction set (Fig. 3 x86), comprising: a first execution controller executing a first decoded result being a decoded signal of an instruction included in the first instruction set; a second execution controller executing a second decoded result being a decoded signal of an instruction included in the second instruction set, the second execution controller being set up independently from the first execution controller (Fig. 3 - *note that the arrows controlling the instructions of particular instruction sets to particular central windows and execution units represent execution controllers - moreover, note that the execution paths are different for different instruction sets; alternatively, the Central Window 20 components can be considered execution*

controllers); a first arithmetic unit (22A-22C) performing an arithmetical operation relative to execution of only the first decoded result (Fig. 3); and a shared arithmetic unit operatively coupled in common to the first and second execution controllers to perform arithmetical operations relative to execution of the first decoded result and the second decoded result (Fig. 3 reference 24A-24B – *note that these units execute both RISC and x86 instructions*).

10. Regarding claim 24, Miller discloses the processor according to claim 23, further comprising: a first decoder that generates the first decoded result by decoding the instruction included in the first instruction set (Fig. 3 reference 18); and a second decoder that generates the second decoded result by decoding the instruction included in the second instruction set (Fig. 3 reference 36; col 5 lines 41-51).

11. Regarding claim 26, Miller discloses the processor according to claim 23, further comprising: a common instruction set decoder that decodes a common instruction included commonly in the first and second instruction sets (Fig. 3). Note that the Instruction Alignment Unit 18 sends instructions to the MROM Unit 36 after completing a determination (col 5 lines 41-51) that is part of the decoding

12. Regarding claim 27, Miller discloses the processor according to claim 24, further comprising: a pipeline stage that is provided between the first decoder and the first processing unit (Fig. 3 reference 20).

13. Regarding claim 28, Miller discloses the processor according to claim 24, further comprising: a first pipeline stage provided between the first decoder and the first processing unit; and a second pipeline stage provided between the second decoder and the second processing unit (Fig. 3 reference 20).

14. Regarding claim 29, Miller discloses the processor according to claim 28, wherein said first pipeline has a different number from said second pipeline (Fig. 3 reference 36 - *a second level of decoding only used for the second pipeline*).

15. Regarding claim 30, Miller discloses the processor according to claim 27, wherein said stage number of the pipeline is variable (Fig. 3 reference 36; col 5 lines 41-51 – *the variability depends on the type of instruction*).

16. Regarding claim 31, Miller discloses the processor according to claim 28, wherein the stage number of the first and second pipelines are variable (Fig. 3 reference 36; col 5 lines 41-51 – *the variability depends on the type of instruction*)..

17. Regarding claim 34, Miller discloses the processor according to claim 24, wherein any one of the first and second decoders is selected for use in response to an interrupt signal (Fig. 3). *Note that a signal (in particular, one interrupting the common*

instruction paths because of a complex signal) is necessary to cause instructions to be sent to the MROM unit 36.

18. Regarding claim 36, Miller discloses the processor according to claim 23, further comprising: a memory that stores both the first and second decoded results (Fig. 3 reference 20).

19. Regarding claim 41, Miller discloses the processor according to claim 23, further comprising: a first register file operating with regard to execution of only the first decoded result; and a shared register file operating with regard to execution of the first decoded result or the second decoded result (col 7 line 32 to col 8 line 3)

20. Regarding claim 42, Miller discloses the processor according to claim 41, further comprising: a second arithmetic unit performing an arithmetical operation relative to execution of only the second decoded result; and a second register file operating with regard to execution of only the second decoded result (fig. 3 references 22A-22C and 40).

21. Regarding claim 47, Miller discloses a processor comprising: a first decoder decoding a first instruction to output a first decoded result without decoding a second instruction (Fig. 3 reference 18); a second decoder decoding the second instruction to output a second decoded result without decoding the first instruction (Fig. 3 reference

36); a first execution controller coupled to the first decoder to transmit a first control signal in response to the first decoded result from the first decoder (Fig. 3 arrows); a second execution controller coupled to the second decoder to transmit a second control signal in response to the second decoded result from the second decoder (Fig. 3 arrows); a first arithmetic unit coupled to the first execution controller to operate with regard to execution of the first decoded result in response to the first control signal (Fig. 3 references 22A-C), said first arithmetic unit being not responsive to the second control signal from the second execution controller (*note that 22A-C do not get inputs from the MROM Unit*); a shared arithmetic unit operatively coupled to the first and second execution controllers to operate with regard to execution of the first and second decoded results in response to one of the first and second control signals (Fig. 3 reference 24A). *Note that the arrows imply the use of some switching multiplexer; the claimed "control signals" are disclosed by the required select signals of those multiplexers.*

22. Regarding claim 48, Miller discloses the processor according to claim 47, further comprising: a second arithmetic unit coupled to the second execution controller to operate with regard to an execution of the second decoded result in response to the second control signal without responding to the first control signal from the first execution controller (Fig. 3 reference 22A-B – *note that these are not responsive to the control signals going into 30-32A-C).*

23. Regarding claim 49, Miller discloses the processor according to claim 47, wherein the first arithmetic unit and the shared arithmetic unit receive the first control signal from the first execution controller at the same time (Fig. 3; col 6 lines 16-20).

24. Regarding claim 50, Miller discloses a data processing system comprising: a first controller coupled to receive a first set of instructions and to provide first control signals (Fig. 3 RISC instructions); a second controller coupled to receive a second set of instructions to provide second control signals (Fig. 3 x86 instructions); a first operation unit (Fig. 3 references 22A-C); a second operation unit (Fig. 3 references 22A-B); a first information transmission path having one node thereof coupled to said first operation unit and another node thereof coupled to said first controller (Fig. 3 RISC path, references 18, 30A-C, 32A-C, 34A-C and 22A-C), said another node of said first information transmission path being independent of said second controller (Fig. 3 references 22A-C contain no x86 instructions); and a second information transmission path having one node thereof coupled to said second operation unit (Fig. 3 reference 36), another node thereof coupled to said first controller (Fig. 3 reference 18) and yet another node thereof coupled to said second controller (Fig. 3 reference 24A-B), said second information transmission path being responsive to an operational mode of said system to couple said one node thereof selectively to one of said another and yet another nodes thereof (Fig. 3 – *note the separate transmission paths*), said first and second operation units being supplied with respective control signals through said

transmission paths to operate respectively (*multiplexer select signals* implied by arrows if Fig. 3).

Claim Rejections - 35 USC § 103

25. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

26. Claims 32, 33 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Trivedi (U.S. Patent No. 6,430,674).

27. Regarding claim 32, Miller discloses the processor according to claim 24, but fails to disclose a system instruction decoder as claimed.

Trivedi discloses the system instruction decoder (Fig. 3 reference 306).

Miller would have been motivated to utilize the technique of having a separate decoder for a system instruction so not to burden the standard pipeline with unique instructions and improve efficiency. These detected system instructions can have several functions, including inducing a low power mode, as shown in col 7 lines 4-7 of Trivedi, thus saving power when it is not needed.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Miller and incorporating a system instruction

with a unique decoder in order to change the mode of the processing into, for example, a low power mode.

28. Regarding claim 33, Miller/Trivedi discloses processor according to claim 32, wherein said system instruction decoder is provided separate from the first and second decoders (Trivedi Fig. 3 reference 306).

29. Regarding claim 35, Miller/ Trivedi discloses the processor according to claim 32, wherein said system instruction includes at least one of instructions for setting power voltage and/or operating rate at which the processor operates (Trivedi col 7 lines 4-7).

Response to Arguments

30. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Brian Johnson/
Examiner, Art Unit 2183

/Aimee J Li/
Primary Examiner, Art Unit 2183